AMENDMENTS TO SPECIFICATION:

Please replace the paragraph beginning on page 7, line 4 with the following amended paragraph:

> "To provide for high speed standard mode, the logic circuit 42 includes hardware or software that recognizes assertion of the Address Enable and Write Enable lines, and automatically addresses registers R1 and R2 sequentially for storing respective data bytes that are placed sequentially on the bus. As will be appreciated by one of ordinary skill in the art, the software instructions may be stored on a machine readable medium."

Please replace the paragraph beginning on page 8, line 21 with the following amended paragraph:

> "For operation in high speed enhanced mode according to the invention, where an upper byte is already present in the register R2 of Figure 2, a first byte is transmitted normally, as described above. However, the first byte will be understood to be the last byte when, subsequently, the CPU de-asserts the Address Enable signal and asserts either the Read Enable or Write Enable signal, indicating a Read or Write Data cycle, for reading to or writing from a memory location. Various ways of implementing this logic, either in hardware or in software, will be readily apparent to persons of ordinary skill. In addition, in the case where this logic is implemented in software, the software may be stored on a machine readable medium."

Please replace the paragraph beginning on page 8, line 14 with the following amended paragraph:

> "The timing diagram of Figure 3 defines the logic used by the logic circuit 42~~-C~~ for determining that the CPU does not intend to send an upper byte UB_2 for a second address A2. For normal operation, that is, where two bytes of address are transmitted, the Address Enable signal is asserted and the Read Enable signal is de-asserted. The Write Enable signal transitions from being asserted to being de-asserted during transmission of the first byte, and transitions again in the same manner during transmission of the second byte."

Please replace the paragraph beginning on page 9, line 9 with the following amended paragraph:

"Particularly, with reference to Figure 4, time t = 0 represents an initial state of the registers R1 and R2, where register R1 contains arbitrary data G1 and R2 contains arbitrary data G2. At a subsequent time t = 1, a lower byte LB_1 over-writes G1 in register R1. At a later time t = 2, an upper byte UB_1 over-writes G2 in register R2. At a still later time t = 3, a new lower byte LB_2 over-writes LB_1 in register R1. Finally, the logic circuit 42~~-C~~ proceeds in high speed enhanced mode, based on the state defined by the Address Enable, Read Enable and Write Enable signals after receipt of the lower byte LB_2, to send the address defined by the two registers to the Control section (Figures 1 and 2) of the memory device, for addressing the location L."